Modular Multilevel DC/DC Converters With Phase-Shift Control Scheme for High-Voltage DC-Based Systems

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***Abstract*—In this paper, by investigating the topology derivation principle of the phase-shift-controlled three-level dc/dc converters, the modular multilevel dc/dc converters, by integrating the full-bridge converters and three-level flying capacitor circuit, are proposed for the high step-down and high power dc-based systems. The high switch voltage stress in the primary side is effectively reduced by the full-bridge modules in series. Therefore, the low-voltage-rated power devices can be employed to obtain the benefits of low conduction losses. More importantly, the voltage autobalance ability among the cascaded modules is achieved by the inherent flying capacitor, which removes the additional possible active components or control loops. In addition, zero-voltage-switching performance for all the active switches can be provided due to the phase-shift control scheme, which can reduce the switching losses. The circuit operation and converter performance are analyzed in detail. Finally, the performance of the presented converter is verified by the simulation and experimental results from a 2-kW prototype.**

***Index Terms*—Input voltage autobalance, modular multilevel dc/dc converter, phase-shift control scheme, zero-voltage switching (ZVS).**

I. Introduction

DC-BASED distributions and dc-based microgrids are recognized as the promising solutions for future smart-grid systems due to their clear advantages of flexibility for photovoltaic and fuel cells interface, without frequency stability, high conversion efficiency, and easy system control [1], [2]. Furthermore, dc-based data center and residential systems have received considerable attention [3], [4]. In general, a high dc voltage is required for the dc-based distribution and microgrid systems to improve the delivery power capability and reduce the transmission losses. Consequently, high-voltage dc/dc converters with high performance are quite attractive and challengeable research topics in the power electronics community.

Manuscript received September 28, 2013; revised December 11, 2013; accepted January 7, 2014. Date of publication January 21, 2014; date of current version August 26, 2014. This work was supported by the National Basic Research Program of China (973 Program 2014CB247400) and the National Nature Science Foundation of China (51222702). Recommended for publication by Associate Editor Z. Xu.

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Digital Object Identifier 10.1109/TPEL.2014.2301722

For the full-bridge-based high power converters, the high-voltage-rated power MOSFETs and insulated-gate bipolar transistors are required to sustain the high bus voltage, which increases the conduction losses and impact the power density owing to the technological limitations of high-voltage semiconductors. In order to reduce the voltage stress on the active switches, some efforts have been made to derive the advanced converter topologies. The series-input series-rectifier interleaved forward converter with a common transformer reset circuit is proposed in [5], which reduces the switch voltage stress to half of that of the conventional active-clamp forward converters. Likewise, a coupled dual interleaved flyback converter is introduced to halve the switch voltage stress compared with the conventional flyback converters in [6]. Unfortunately, their hard switching operation impacts the conversion efficiency. Furthermore, the interleaved resonant converters with series-connected transformers are given in [7] and [8]. The series half-bridge cells can reduce the switch voltage stress. However, some transformers with multiple windings exist. Moreover, the series asymmetrical half-bridge converter is presented in [9], which combines two asymmetrical half-bridge cells and shares the same transformer and leakage inductance. In addition, three pairs of series switches are connected in the primary side in [10], which reduces the switch voltage stress to only one-third of the high input voltage. In [11], the auxiliary snubber circuit is added to achieve ZVS in a wide load range and reduce the circulating current. Aforementioned topology in [10] is extended to N pairs of half-bridge cells in [12], where the voltage stress of the primary switches is only one Nth of the high input voltage. However, the input voltage autobalance mechanism does not exist, which means that additional balance circuits or voltage-sharing control loops are necessary. Three-level converters (TLCs) are appropriate candidates in the high input voltage applications for the advantage of automatically half-input voltage stress on the switches [13]. In order to extend the soft-switching range for the primary switches or minimize the reverse-recovery losses for the secondary diodes, some state-of-the-art improvements are generated [14], [15]. Furthermore, multilevel converters with more devices can span higher input voltage. Unfortunately, the number of the achievable voltage levels is quite limited not only due to the voltage unbalance problems but also due to the voltage clamping requirements, circuit layout, and packaging constraints [16].

The input-series output-parallel (ISOP) connected modular converters are regarded as good choices in the high input voltage

applications. Besides the advantage of the switch voltage stress reduction, ISOP converters are the important step toward truly modular power converter architecture, where the low-power, low-voltage, standardized modules can be connected to realize any given system specifications [17]. However, the input voltage balance is critical for the ISOP systems. Common duty ratio control scheme is proposed in [17] and [18], where the same duty ratio signal is applied to the different modules, and then the input voltage sharing is theoretically achieved, but equally to the extent that the other parameters are equal. Many kinds of control strategies [19]–[24] are carried out to optimize the input voltage balance performance, but the complexity and cost of the system are increased.

In this paper, the flying capacitor and full-bridge converters are combined and integrated to derive the advanced modular multilevel dc/dc converters for the high step-down and high power dc-based conversion applications. Due to the charging and discharging balance of the built-in flying capacitor, the input voltage autobalance ability is naturally realized, which halves the switch voltage stress and overcomes the input voltage imbalance. Furthermore, the phase-shift control strategy can be adopted to achieve the soft-switching operation and reduce the switching losses. The concept of modular multilevel dc/dc converters may provide a clear picture on high-voltage dc/dc topologies for the dc-based distribution and microgrid systems.

The outline of this paper is highlighted as follows. The derivation law of the proposed modular multilevel dc/dc converters is illustrated in Section II. The operational principle and the input voltage autobalance mechanism are analyzed in Section III. Besides, the circuit characteristics of the proposed converter are specified in Section IV. The performance of the presented converter is verified by the simulation and experimental results from the built 2-kW prototype in Section V. The main contributions of this paper are summarized in the last section.

II. Derivation Law of Modular Multilevel Converters

The derivation process of the proposed modular multilevel dc/dc converters is discussed in this section. It is well known that the neutral-point-clamped (NPC) converters and flying capacitor-based converters are the major multilevel topologies for the high-voltage and high-power applications [25]. For the conventional NPC converters with pulse width modulation control, the abnormal operation condition, such as the mismatch in the gate signals, may cause the voltage imbalance of the input capacitors. Therefore, the converter reliability is impacted. Furthermore, the phase-shift control scheme is not suitable for the conventional NPC converters, which leads to large switching losses. Fortunately, by inserting a small flying capacitor parallel connected with the clamping diodes, the input capacitor voltages are automatically shared because the flying capacitor can be directly parallel with the series input capacitors alternatively [26]. More importantly, the phase-shift control strategy can be easily applied to achieve zero-voltage-switching (ZVS) operation without adding any other power components. The phase-shift-controlled three-level dc/dc converter is plotted in Fig. 1(c). From another point of view, the phase-shift-controlled TLC can

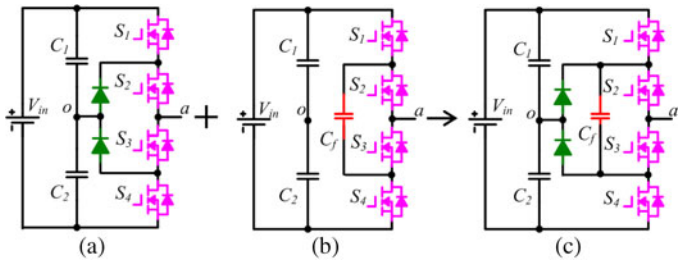

Fig. 1. Derivation of novel TLC: (a) NPC TLC, (b) flying capacitor-based TLC, and (c) phase-shift-controlled combined TLC.

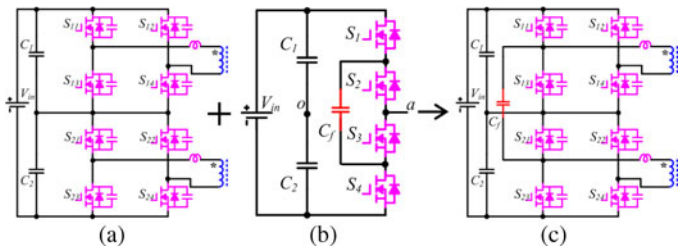

Fig. 2. Derivation of the proposed modular multilevel dc/dc converter: (a) cascaded full-bridge converter, (b) flying capacitor-based TLC, and (c) proposed modular multilevel dc/dc topology.

be regarded as the combination and integration of the three-level NPC converter as given in Fig. 1(a) and the three-level flying capacitor-based circuit as shown in Fig. 1(b), where the input capacitors and active power switches are reused and shared to reduce the circuit complexity. As a result, the advantages of the NPC converter and flying capacitor-based circuit are kept whereas their inherent disadvantages are effectively avoided. Many further improvements are made for the combined phase-shift-controlled TLC by adding some active or passive components to extend the soft-switching operation range [26]–[36].

Based on the previously summarized combined multilevel derivation principle, it is innovative and attractive to consider the possibility of combination of the other fundamental multilevel topologies. For example, the cascaded full-bridge converter, or the ISOP full-bridge converter, and the three-level flying capacitor-based converter are combined and integrated to derive the advanced modular multilevel dc/dc converters, which is detailed illustrated in Fig. 2. The time sequence of the leading leg in the phase-shift-controlled full-bridge converters is kept constant and only the phase of the lagging leg is shifted to regulate the output voltage. This indicates that the leading legs of the cascaded full-bridge converter can be assembled with the three-level flying capacitor-based converter to achieve the input voltage autobalance. And the lagging legs of the cascaded full-bridge converter are still kept unchanged to provide adequate control freedom to achieve fast and accurate output voltage regulation. Consequently, for the proposed modular multilevel dc/dc converters, the big concern of the input-voltage imbalance existed in the ISOP converters is completely overcome due to the built-in flying capacitor. More importantly, the derived modular multilevel dc/dc concept can be easily put forward to N-stage converters by stacking the full-bridge power modules in series in the primary side to satisfy the growing bus voltage

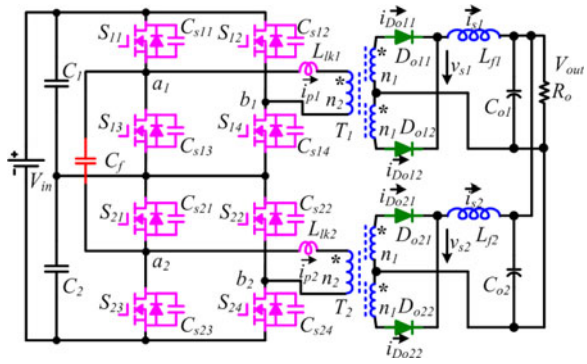

Fig. 3. Proposed modular multilevel dc/dc converter with input voltage autobalance ability.

in the dc-based distribution and microgrid systems. In view of the phase-shift-controlled topologies, the aforementioned optimized strategies for the phase-shifted-controlled TLCs can be directly transferred to the derived modular multilevel dc/dc converters to generate a family of high performance topologies for the high-voltage and high-power applications. It can be concluded that this modular multilevel converter concept is one of the general solutions for the high-voltage and high-power dc/dc topology origination.

III. Operation Principle and Input Voltage Autobalance Mechanism

For the secondary side of the derived modular multilevel dc/dc converters, the current-type full-wave rectifier, full-bridge rectifier, current doubler rectifier, and other advanced current-type rectifiers can be employed. In this section, the widely adopted current-type full-wave rectifier is applied as an example to explore the circuit performance of the proposed modular multilevel configuration, which is illustrated in Fig. 3. In the primary side, the capacitors C_1 and C_2 are used to split the high input voltage, $S_{11}-S_{14}$ are the power switches of the top full-bridge module, $S_{21}-S_{24}$ form the bottom full-bridge module, $C_{s11}-C_{s24}$ are the parasitic capacitors of the power switches, and L_{lk1} and L_{lk2} are the leakage inductors of the transformers T_1 and T_2, respectively. In the secondary side, D_{o11}, D_{o12}, L_{f1}, and C_{o1} are for the top full-bridge module and D_{o21}, D_{o22}, L_{f2}, and C_{o2} are for the bottom full-bridge module. $i_{p1}, i_{p2}, i_{\mathrm{Do11}}, i_{\mathrm{Do12}}, i_{\mathrm{Do21}}$, and i_{Do22} are the primary and secondary currents through the windings of the transformers with the defined direction in Fig. 3. And i_{s1} and i_{s2} are the filter inductors currents.

A. Operation Analysis

The phase-shift control scheme is employed in the proposed converter to realize the ZVS performance of all the power switches, where S_{11}, S_{13}, S_{21}, and S_{23} are the leading-leg switches and S_{12}, S_{14}, S_{22}, and S_{24} are the lagging-leg switches. The key waveforms of the proposed converter are shown in Fig. 4. For the top full-bridge module, S_{11} and S_{13} act with 0.5 duty cycle complementarily with proper dead time t_d, so as for the switches S_{12} and S_{14}. The phase-shift angle between the leading and lagging switch pairs is defined as φ_1.

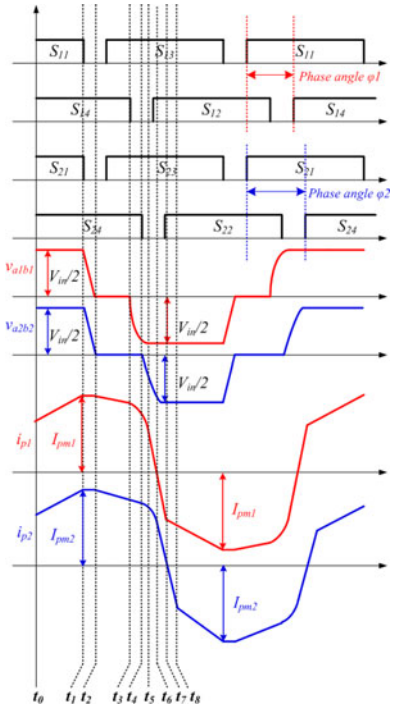

Fig. 4. Key waveforms of the proposed converter.

The gate signal pattern of the bottom full-bridge module is similar to that of the top full-bridge module with the phase-shift angle φ_2. Meanwhile, the leading switches pair S_{11} and S_{13} turns ON and OFF simultaneously with the switch pair S_{21} and S_{23}, while the phase-shift angles φ_1 and φ_2 are decoupled control freedoms for the output voltage regulation. The mode 0 $< \varphi_1 - \varphi_2 < t_d$ is taken into consideration when analyzing the operation of the converter, and the equivalent operation circuits are depicted in Fig. 5.

In order to simplify the analysis, the following assumptions are made: 1) all the power switches and diodes are ideal; 2) the parasitic capacitors $C_{s11}-C_{s24}$ of the switches have the same value as C_s; 3) the voltage ripples on the divided input capacitors C_1, C_2 and flying capacitors C_f are small due to their large capacitance; 4) the turns ratio of both transformers is $N = n_2{:}n_1$; and 5) the input voltage is balanced and the autobalance mechanism will be depicted later. There are 15 operation stages in one switching period. Due to the symmetrical circuit structure and operation, only the first eight stages are analyzed as follows.

Stage 1 [t_0, t_1]: Before t_1, the switches S_{11}, S_{14}, S_{21}, and S_{24} are in the turn-on state to deliver the power to the secondary side. The output diodes D_{o11} and D_{o21} are conducted and the output diodes D_{o12} and D_{o22} are reverse biased. The flying capacitor C_f is in parallel with the input divided capacitor C_1 to make V_{Cf} equal to V_{C1}. The primary currents i_{p1} and i_{p2} are expressed as follows, which is increased to the peak value at the end of this stage:

$$i_{p1}(t) = i_{p1}(t_0) + \frac{V_{\mathrm{in}}/2 - NV_{\mathrm{out}}}{L_{lk1} + N^2 L_{f1}}(t - t_0) \tag{1}$$

$$i_{p2}(t) = i_{p2}(t_0) + \frac{V_{\mathrm{in}}/2 - NV_{\mathrm{out}}}{L_{lk2} + N^2 L_{f2}}(t - t_0). \tag{2}$$

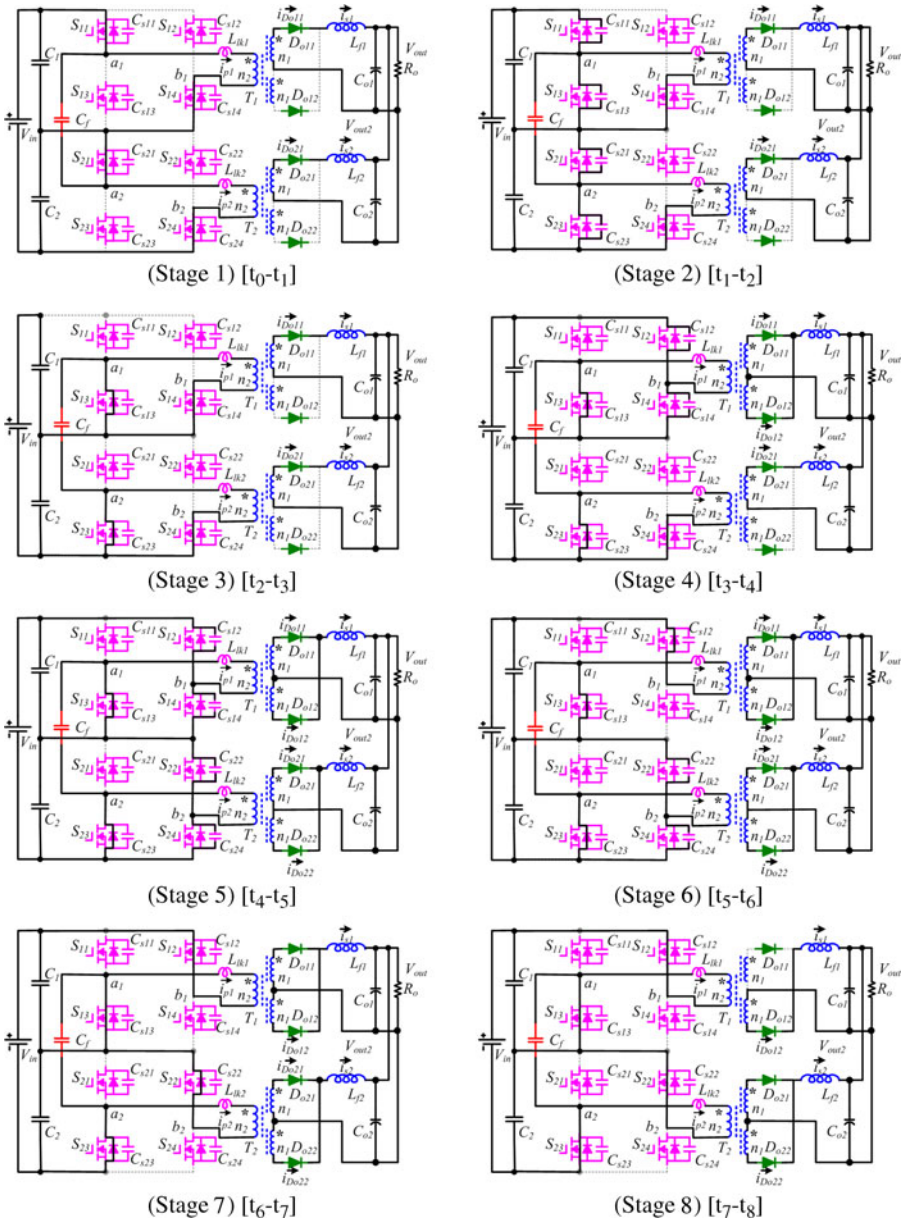

Fig. 5. Equivalent operation circuits of the proposed converter. (Stage 1) [t_0–t_1], (Stage 2) [t_1–t_2], (Stage 3) [t_2–t_3], (Stage 4) [t_3–t_4], (Stage 5) [t_4–t_5], (Stage 6) [t_5–t_6], (Stage 7) [t_6–t_7], and (Stage 8) [t_7–t_8]

Stage 2 [t_1, t_2]: At t_1, the turn-off signals of the switches S_{11} and S_{21} are given. ZVS turn off for these two switches are achieved due to the capacitors C_{s11} and C_{s21}. C_{s11} and C_{s21} are charged and C_{s13} and C_{s23} are discharged by the primary currents.

Stage 3 [t_2, t_3]: At t_2, the voltages of C_{s13} and C_{s23} reach 0 and the body diodes of S_{13} and S_{23} are conducted, providing the ZVS turn-on condition for S_{13} and S_{23}. The flying capacitor C_f is changed to be in parallel with the input divided capacitor C_2. The primary currents are derived by

$$i_{p1}(t) = \frac{i_{s1}(t)}{N} \tag{3}$$

$$i_{p2}(t) = \frac{i_{s2}(t)}{N}. \tag{4}$$

Stage 4 [t_3, t_4]: At t_3, S_{14} turns off with ZVS. C_{s14} is charged and C_{s12} is discharged, leading to the forward bias of D_{o12}; hence, the secondary current i_{s1} circulates freely through both D_{o11} and D_{o12}. i_{p1} is regulated by

$$i_{p1}(t) = i_{p1}(t_3)\cos\omega(t - t_3) \tag{5}$$

where

$$\omega = \frac{1}{\sqrt{2L_{lk2}C_s}}. \tag{6}$$

Stage 5 [t_4, t_5]: At t_4, the turn-off signal of S_{24} comes. ZVS turn-off performance is achieved for S_{24}. Similar to the previous time interval, D_{o21} and D_{o22} conduct simultaneously, thus leading to the transformer T_2 short-circuit. i_{p2} is regulated by

$$i_{p2}(t) = i_{p2}(t_4)\cos\omega(t - t_4) \tag{7}$$

TABLE I
EFFECT OF DIFFERENT FACTORS

Cases	Results of unbalanced voltage
$N_1>N_2$	$V_{C1}>V_{C2}$
$L_{lk1}>L_{lk2}$	$V_{C1}>V_{C2}$
$\varphi_1>\varphi_2$	$V_{C1}>V_{C2}$

where

$$\omega = \frac{1}{\sqrt{2L_{lk2}C_s}}. \tag{8}$$

Stage 6 [t_5, t_6]: At t_5, C_{s12} is discharged completely and the antiparallel diode of S_{12} conducts, getting ready for the ZVS Turn-on of S_{12}. During this time interval, i_{p1} declines steeply duo to half-input voltage across the leakage inductor L_{lk1}. i_{p1} is given by

$$i_{p1}(t) = i_{p1}(t_5) - \frac{V_{\text{in}}/2}{L_{lk1}}(t - t_5). \tag{9}$$

Stage 7 [t_6, t_7]: At t_6, i_{p1} decreases to 0 and increases reversely with the same slope through S_{12} and S_{13}. C_{s22} is discharged completely and the antiparallel diode of S_{22} conducts. i_{p2} declines rapidly duo to half-input voltage across the leakage inductor L_{lk2}. i_{p2} is given by

$$i_{p2}(t) = i_{p2}(t_6) - \frac{V_{\text{in}}/2}{L_{lk2}}(t - t_6). \tag{10}$$

Stage 8 [t_7, t_8]: At t_7, i_{p2} decreases to 0 and increases reversely through S_{22} and S_{23}. The current through the output diode D_{o11} decreases to 0 and turns off. The output diode D_{o21} turns off after t_8, and then a similar operation works in the rest stages.

B. Input Voltage Autobalance Mechanism

The input voltage imbalance is one of the major drawbacks for most multilevel converters and ISOP converters, which is mainly caused by the asymmetry of the component parameter difference and the mismatch of control signals. It has been carried out that the transformer turns ratio difference (N), leakage inductance distinction (L_{lk}), and phase-shift angle mismatch (φ) are the main reasons for the input voltage imbalance in the steady state for the ISOP phase-shift-controlled converters [18]. The effect of these factors is summarized in Table I, which shows that $N_1 > N_2$ or $L_{lk1} > L_{lk2}$ or $\varphi_1 > \varphi_2$ leads to the voltage V_{C1} on the top input capacitor C_1 higher than the voltage V_{C2} on the bottom capacitor C_2 and vice versa. As the parameter difference increases, the voltage gap between V_{C1} and V_{C2} increases correspondingly.

The input voltage autobalance mechanism of the proposed modular multilevel dc/dc converter is displayed in Fig. 6 and detailed elaborated as follows. According to the steady operation of the proposed converter, for the leading-leg switches,

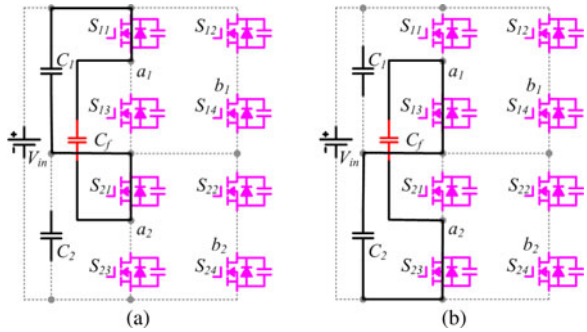

Fig. 6. Input voltage autobalance mechanism: (a) C_f in parallel with C_1 and (b) C_f in parallel with C_2.

the switches S_{11} and S_{21} have the same time sequence and the switches S_{13} and S_{23} are operated synchronously. When S_{11} and S_{21} are turned ON, S_{13} and S_{23} are turned OFF accordingly, and the flying capacitor C_f is connected in parallel with the top input capacitor C_1 as plotted in Fig. 6(a). This makes V_{Cf} equal to V_{c1}. In the same way, as given in Fig. 6(b), the flying capacitor C_f is in parallel with the bottom input capacitor C_2, when S_{13} and S_{23} are in turn-on state. This denotes that V_{Cf} and V_{c2} are the same. The connection of C_f with C_1 or C_2 alternates with high switching frequency, which leads to the voltages on both the input capacitors automatically shared and balanced.

It is important to point out that the flying capacitor does not connect with the lagging-leg switches directly. As a result, the operation of C_f hardly affects the states of the lagging-leg switches. Then, both the two phase-shift angles φ_1 and φ_2 can be taken as control freedoms to regulate the output voltage.

IV. CONVERTER PERFORMANCE ANALYSIS

A. Voltage Stresses of Switches

In the primary side, the voltage stress of the power switches $S_{11} - S_{24}$ is half of the input voltage owing to the series structure and the autobalance mechanism. As a result, the low-voltage-rated power devices are available in the high input applications to restrict the conduction losses.

B. ZVS Soft-Switching Condition

1) Leading Legs: ZVS turn-off is achieved for the leading switches due to their intrinsic capacitors. In order to realize ZVS turn-on, enough energy is needed to charge and discharge the intrinsic capacitors. During the dead time interval $[t_1 - t_2]$, S_{11} and S_{21} are turned OFF; C_{s11} and C_{s21} are charged and C_{s13} and C_{s23} are discharged as shown in Fig. 7. According to the Kirchhoffs law, the following equations are derived:

$$i_{Cs11} + i_{Cs13} = i_{p1} - i_{Cf} \tag{11}$$

$$i_{Cs21} + i_{Cs23} = i_{p2} + i_{Cf}. \tag{12}$$

It is reasonable to assume that i_{p1} and i_{p2} are nearly constant during this period due to the short dead time. When the sum of V_{Cs13} and V_{Cs21} is not equal to V_{Cf}, C_f may be charged

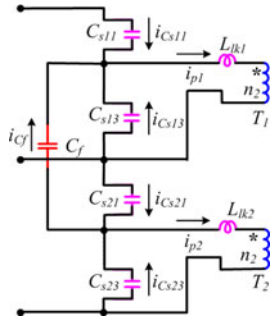

Fig. 7. ZVS equivalent circuit of leading switches during dead time.

or discharged. The current i_{Cf} affects the ZVS performance of the power switches according to (11) and (12): 1) when C_f is discharged, i_{Cf} flows in the positive direction as shown in Fig. 7, and ZVS performance of S_{21} and S_{23} is improved but deteriorated for S_{11} and S_{13}; and 2) when C_f is charged, i_{Cf} flows reversely, which improves the ZVS performance of S_{11} and S_{13} but deteriorates that of S_{21} and S_{23}. Fortunately, C_f is much larger than C_s, making i_{Cf} small. Besides, the output filter inductance is reflected to the primary side and is in series with the resonant inductance. The energy of both the filter inductors and the resonant inductors is sufficient to achieve ZVS for the leading switches. The output filter inductance is so large enough that the leading switches can realize ZVS turn-on even at light loads.

2) Lagging Legs: Similar with the leading switches, the lagging switches are able to realize ZVS turn-off by utilizing their intrinsic capacitors. However, only the energies of the resonant inductors are employed to achieve ZVS turn-on for the lagging switches. In order to accomplish ZVS, the following equation should be satisfied [31]

$$\frac{1}{2}L_{lk}\left(\frac{I_o}{N}\right)^2 > \frac{1}{2}\cdot 2C_s\left(\frac{1}{2}V_{\text{in}}\right)^2 = \frac{1}{4}C_s V_{\text{in}}^2. \tag{13}$$

As the resonant inductance is quite smaller than the filter inductance, the achievement of the ZVS turn-on for the lagging switches is more difficult than the leading switches at light loads.

C. Duty Cycle Loss

During interval [t_3–t_7], V_{a1b1} is negative, and i_{p1} transits from the positive direction to the negative reflected filter inductance current. The secondary diodes D_{o11} and D_{o12} conduct simultaneously, making the secondary rectified voltage become 0. The duty cycle is lost during this time interval, the expression of which is derived by [31]:

$$D_{\text{loss1}} = \frac{2(t_7 - t_3)}{T_s} \approx \frac{8L_{lk1}I_{o1}}{NV_{\text{in}}}. \tag{14}$$

For the bottom full-bridge module, the duty cycle loss is similar to the top full-bridge module as given by

$$D_{\text{loss2}} = \frac{2(t_8 - t_4)}{T_s} \approx \frac{8L_{lk2}I_{o2}}{NV_{\text{in}}} \tag{15}$$

where I_{o1} and I_{o2} are the average output currents of top and bottom full-bridge modules, respectively.

TABLE II
SIMULATION RESULTS

C_f	Variables				Results		
	ΔL_{lk} (μH)	N_1	N_2	$\Delta\varphi$ (°)	V_{c1} (V)	V_{c2} (V)	ΔV (V)
Without	10	18:6:6	18:6:6	0	313.5	286.5	27
	0	18:6:6	16:6:6	0	312.3	287.7	24.6
	0	18:6:6	18:6:6	10	315.8	284.2	31.6
	10	18:6:6	16:6:6	10	343.8	256.2	87.6
With	***10***	***18:6:6***	***16:6:6***	***10***	***300***	***300***	***0***

From the aforementioned analysis, several clear advantages of the proposed modular multilevel dc/dc converter are obtained, which are listed as follows:

1) the voltage stresses of all the primary switches are only half of the input voltage due to the series structure and the input voltage autobalance mechanism;
2) ZVS soft-switching performance is achieved for all of the power switches without any extra active or passive components due to the phase-shift control scheme;
3) the input voltage autobalance is achieved by the flying capacitor without any auxiliary circuits or complex controls;
4) the modular structure of the proposed converter provides the possibility of truly modular system with extended N-stage modules to tackle with higher input voltage.

However, the circulating current at the freewheeling stage is still existed and the ZVS for the lagging switches is difficult at light load in the proposed modular multilevel dc/dc converter. Fortunately, some state-of-the-art improvements for circulating current suppression and soft-switching range extension can be directly transferred to the proposed modular multilevel converter to enhance the circuit performance [26]–[30].

V. Simulation and Experimental Verifications

A. Simulation Verification

In order to investigate the influence of the parameter difference and the control mismatch on the input voltage imbalance, some simulation results are executed as given in Table II. The variables are the leakage inductors, transformer turns ratios, and phase-shift angles. $\Delta L_{lk} = L_{lk1} - L_{lk2}$, N_1 and N_2 are the transformer turns ratios of T_1 and T_2, respectively, and $\Delta\varphi = \varphi_1 - \varphi_2$. The input voltage is 600 V, and the results of the voltage gap ($\Delta V = V_{C1} - V_{C2}$) are revealed in Table II. Fig. 8 shows the simulation waveforms of the last two rows of Table II.

1) Without Flying Capacitor C_f: When $\Delta L_{lk} = 10$ μH, $N_1 = N_2$, $\Delta\varphi = 0°$, V_{c1} is 313.5 V, and V_{c2} is 286.5 V. The voltage difference ΔV is 27 V. Similarly, when only the transformer turns ratios or the phase-shift angles are different to some degree, the voltage gaps are about 24.6 or 31.6 V. However, if the three factors work at the same time, the worst voltage difference can be as large as 87.6 V without any compensation. This

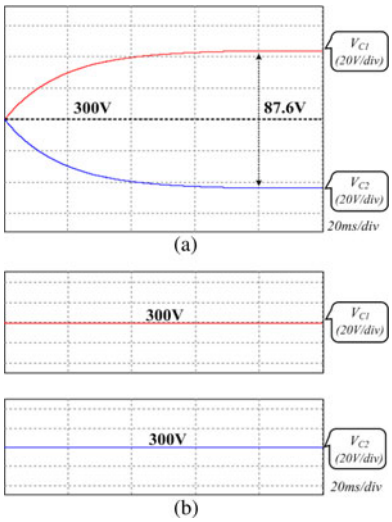

Fig. 8. Simulation waveforms: (a) input voltage without a flying capacitor and (b) input voltage with a flying capacitor.

TABLE III
UTILIZED COMPONENTS AND PARAMETERS OF THE TESTED PROTOTYPE

Components	Parameters
V_{in} (Input voltage)	600 V
V_{out} (Output voltage)	48 V
P_{out} (Maximum output power)	2000 W
f_s (Switching frequency)	100 kHz
$N_1 = N_2$ (Turns ratio = $n_2/n_1/n_1$)	18:6:6
L_{lk1} (Resonant inductance of top full-bridge module)	19.7 μH
L_{lk2} (Resonant inductance of bottom full-bridge module)	19.8 μH
L_{f1} (Filter inductance of top full-bridge module)	37.2 μH
L_{f2} (Filter inductance of bottom full-bridge module)	40.0 μH
$C_1 = C_2$ (Input filter capacitors)	440 μF
C_f (Flying capacitor)	4.75 μF
$C_{o1} = C_{o2}$ (Output filter capacitors)	220 μF
$S_{11} \sim S_{24}$ (Primary power MOSFETs)	IRFP460
$D_{o11} \sim D_{o22}$ (Output diodes)	MUR3040

indicates that the parameter mismatch may lead to the system failure if the appropriate control loops are not adopted.

2) With Flying Capacitor C_f: From Table II, when the three factors work synchronously, the proposed modular multilevel converter shares the input voltage excellently due to the built-in input voltage autobalance mechanism. The input voltage autobalance performance of the proposed converter is also exhibited in Fig. 8 compared with the converter without the flying capacitor.

B. Experimental Verification

In order to verify the performance of the proposed converter, a 2-kW experimental prototype is built and tested. The circuit parameters are listed in Table III.

It is necessary to explicate the design principle of the flying capacitor C_f in this experimental prototype. Charge rate and voltage ripple of the flying capacitor are considered. In order to complete charge and discharge of the C_f during the switching

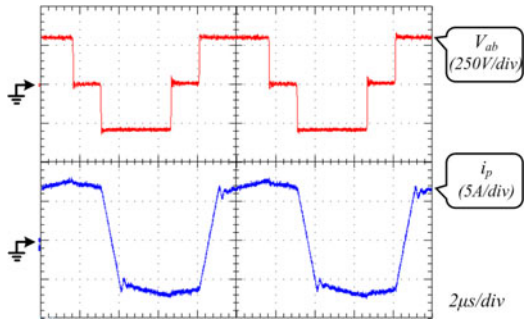

Fig. 9. Experimental result of primary voltage and current.

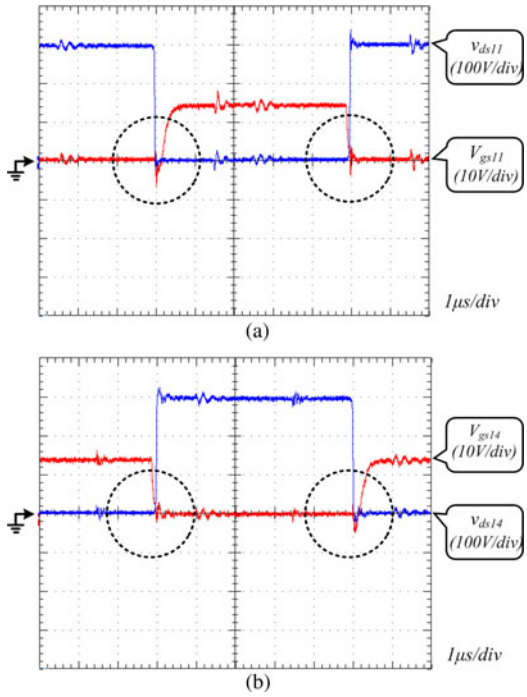

Fig. 10. Experimental result of ZVS operation: (a) ZVS operation for S_{11} and (b) ZVS operation for S_{14}.

period, the following equation should be satisfied:

$$5RC \leq T_s \tag{16}$$

where R is the sum of the resistance of the charge and discharge circuit loop and C is the series of C_f with C_1 or C_2. The voltage ripple of C_f is designed to be limited to 1% in this prototype, so C_f should be large enough to meet the voltage ripple requirements. By simulating, the value of the flying capacitor can be obtained with the tradeoff between the charge rate and the voltage ripple.

The experimental results of the primary input voltage V_{a1b1} and the current i_{p1} at full load are shown in Fig. 9. The voltage waveform is clear without obvious spikes due to the ZVS soft switching of the power switches. The primary current is smooth with slight spikes caused by the resonance between the switches inherent capacitors and the resonant inductance.

The experimental results of the gate signals and the drain–source voltages of the leading switch S_{11} and lagging switch S_{14} are displayed in Fig. 10(a) and (b), respectively. The switch voltage stress is only 300 V, which is half of the input voltage,

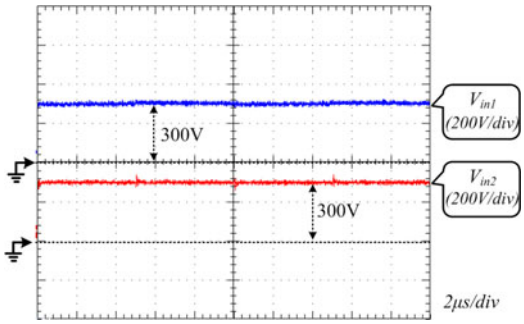

Fig. 11. Experimental result of input voltage sharing.

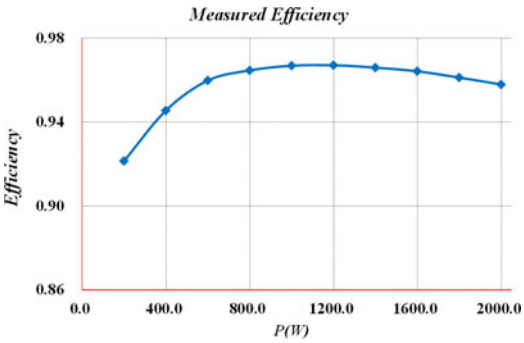

Fig. 12. Measured efficiency of the proposed converter.

indicating that the input voltage sharing is achieved. In addition, ZVS performance for both the leading and lagging switches is realized, which minimizes the switching losses.

Fig. 11 exhibits the input voltage across C_1 and C_2, both of which are 300 V. It can be seen that the input voltage autobalance is accomplished excellently.

The measured efficiency of the proposed converter under different loads condition is plotted in Fig. 12. The maximum efficiency reaches 96% and the efficiency is above 94% over a wide load range.

VI. Conclusion

In this paper, a novel phase-shift-controlled modular multilevel dc/dc converter is proposed and analyzed for the high input voltage dc-based systems. Due to the inherent flying capacitor, which connects the input divided capacitors alternatively, the input voltage is automatically shared and balanced without any additional power components and control loops. Consequently, the switch voltage stress is reduced and the circuit reliability is enhanced. By adopting the phase-shift control scheme, ZVS soft-switching performance is ensured to reduce the switching losses. The modular multilevel dc/dc converter concept can be easily extended to N-stage converter with stacked full-bridge modules to satisfy extremely high-voltage applications with low-voltage-rated power switches.

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